

Fig. 1 (Prior Art)

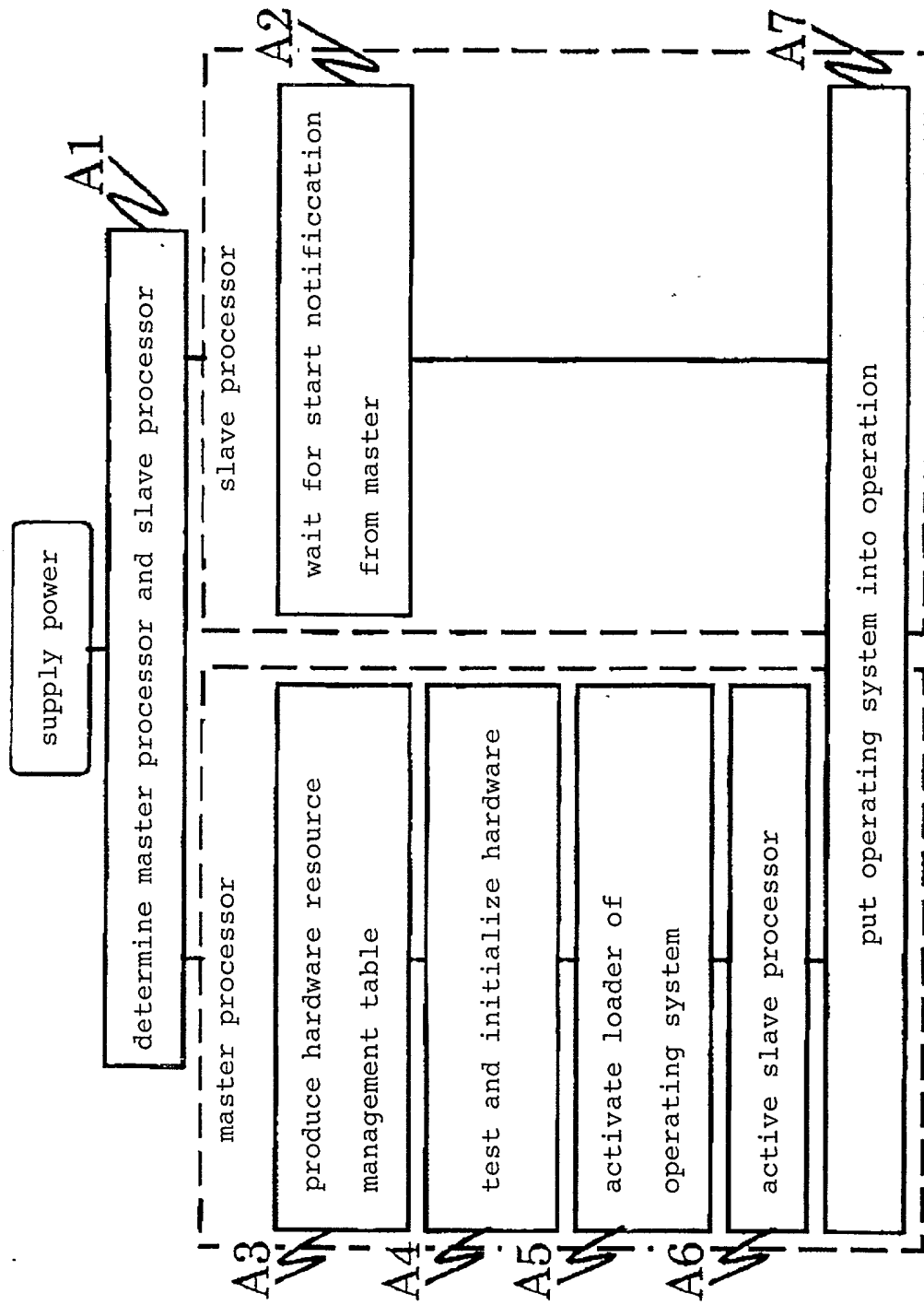


Fig. 2

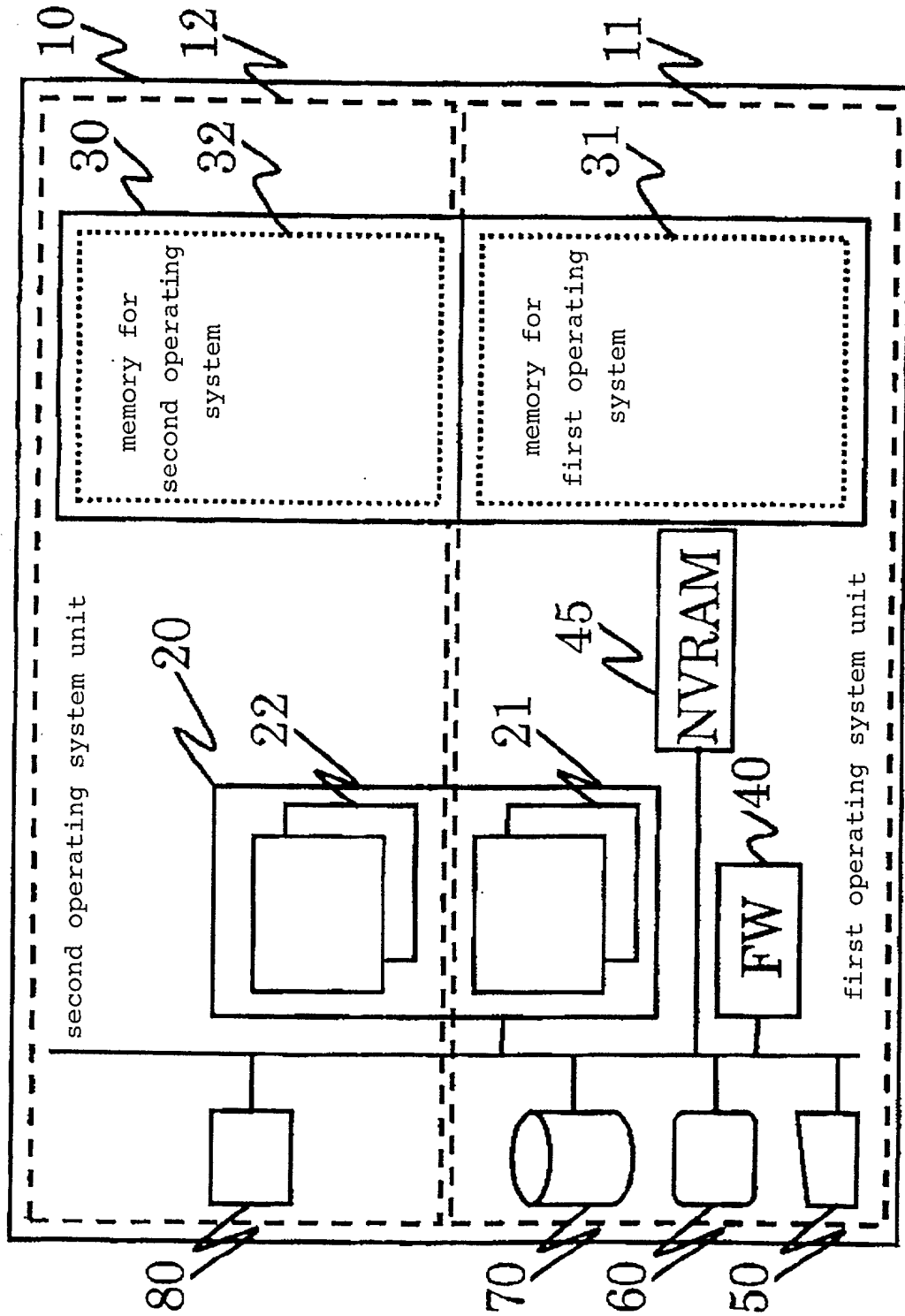


Fig. 3

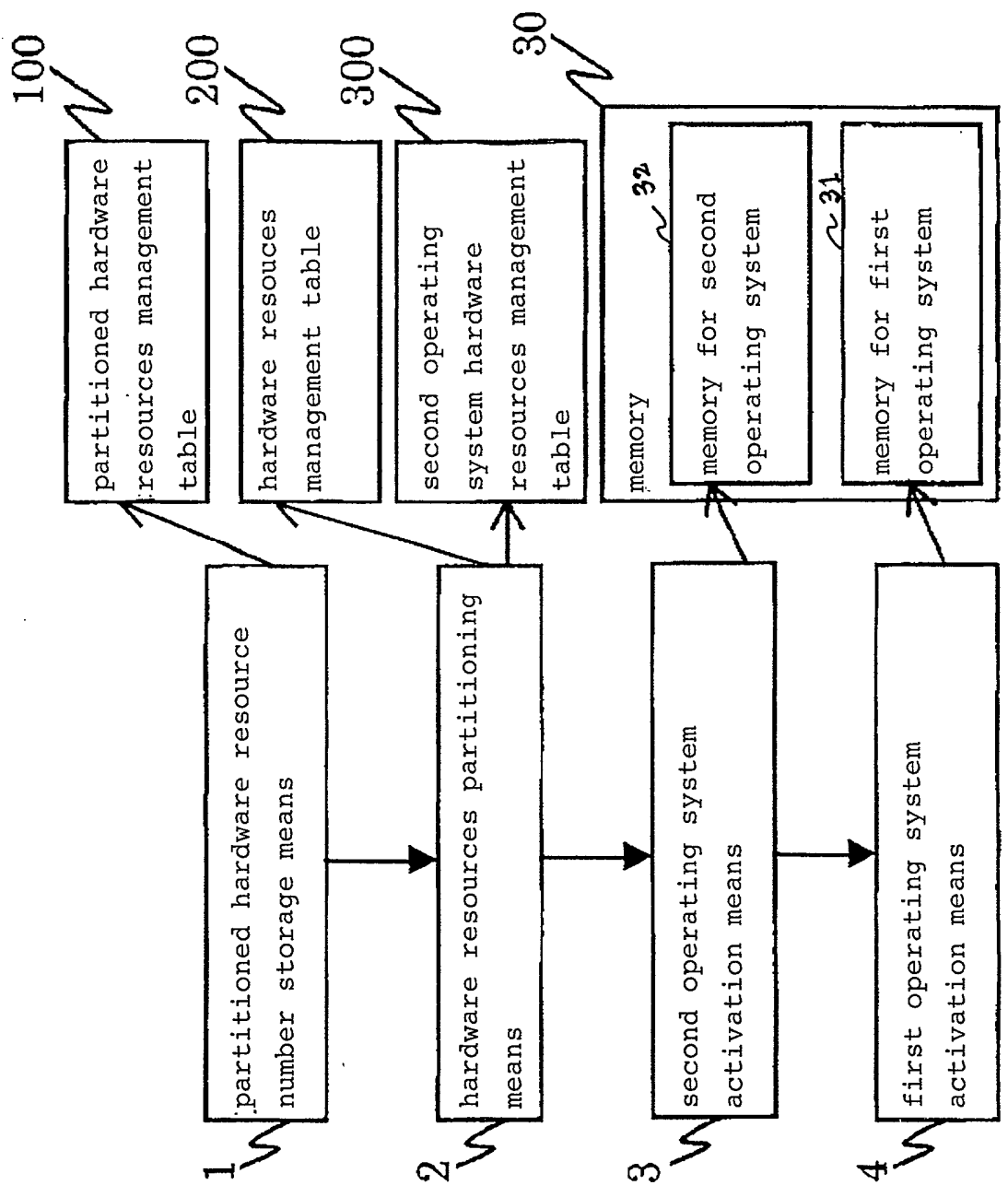


Fig. 4

100	
hardware resources	quantities
processor entry for second operating system	2
interruption entry for second operating system	80
memory entry for second operating system	256MB

Fig. 5

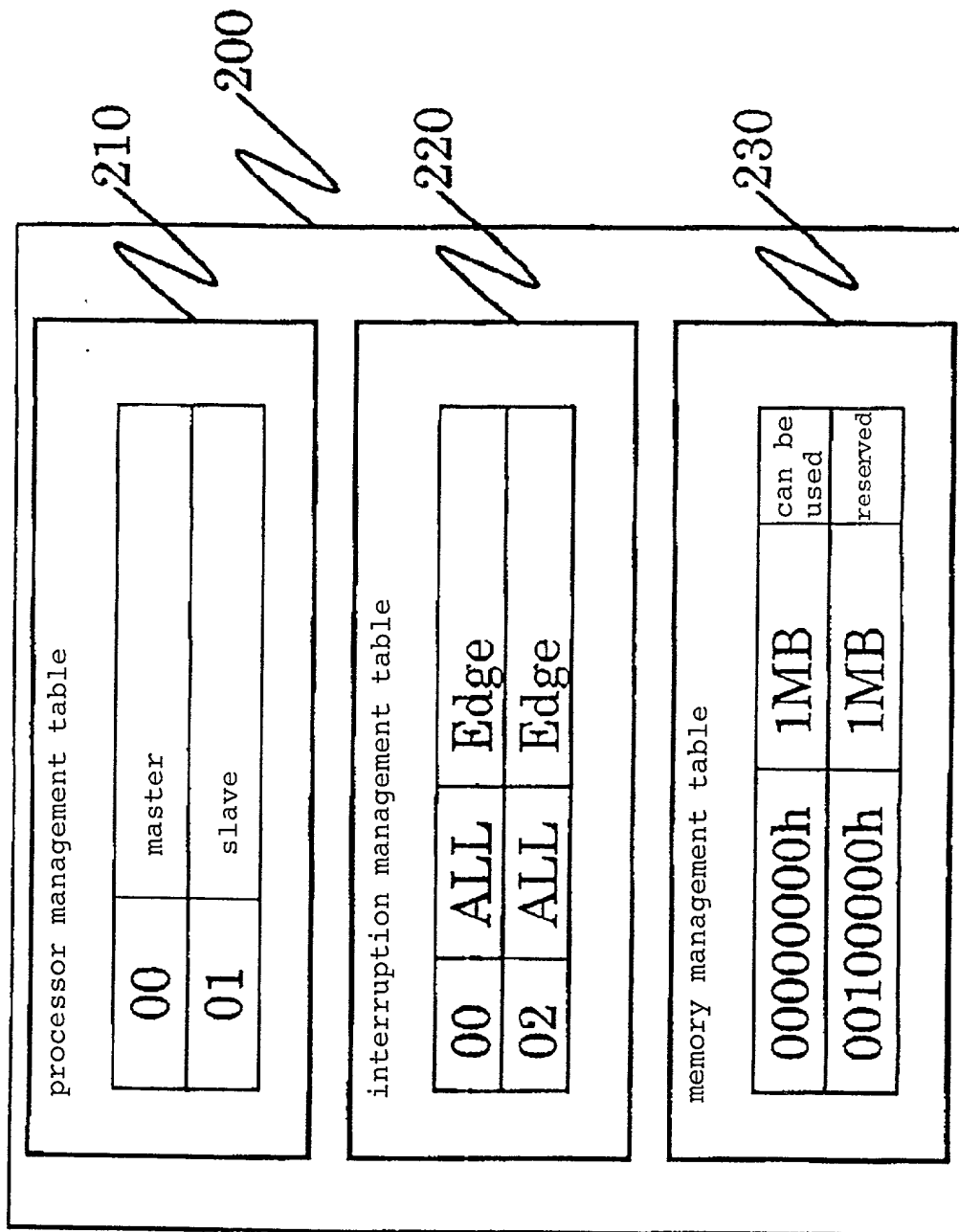


Fig. 6

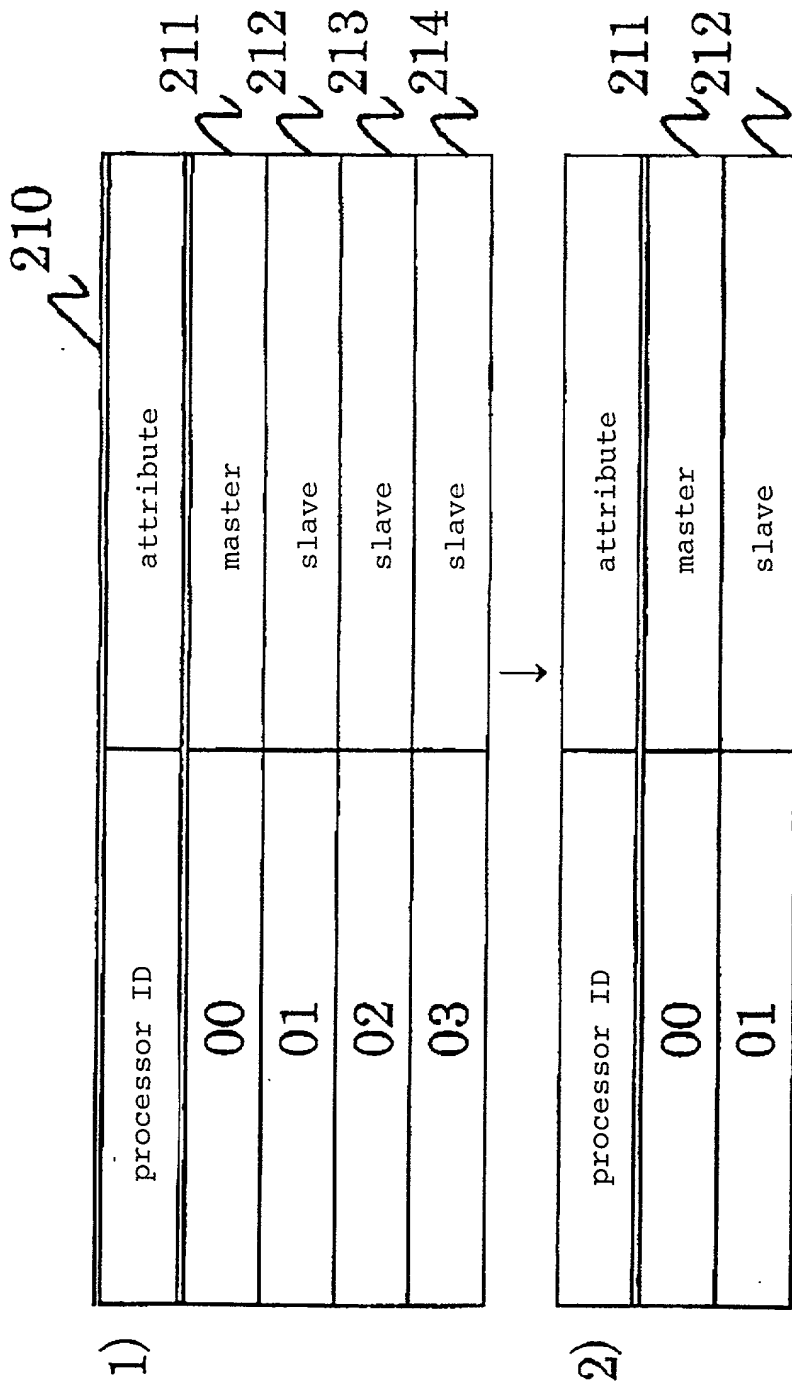


Fig. 7

220

1)

device ID	interruption number	report destination	attribute
50	01	all	edge trigger
60	05	all	edge trigger
80	10	all	level trigger
70	06	all	edge trigger

221 222 223 224

↓

2)

device ID	interruption number	report destination	attribute
50	01	all	edge trigger
60	05	all	edge trigger
70	06	all	edge trigger

221 222 224

Fig. 8

1)	start address	length	attribute	231
	00000000h	1MB	can be used	232
	00100000h	1MB	reserved	233
	00200000h	510MB	can be used	
				↓
2)	start address	length	attribute	231
	00000000h	1MB	can be used	232
	00100000h	1MB	reserved	233
	00200000h	254MB	can be used	

Fig. 10

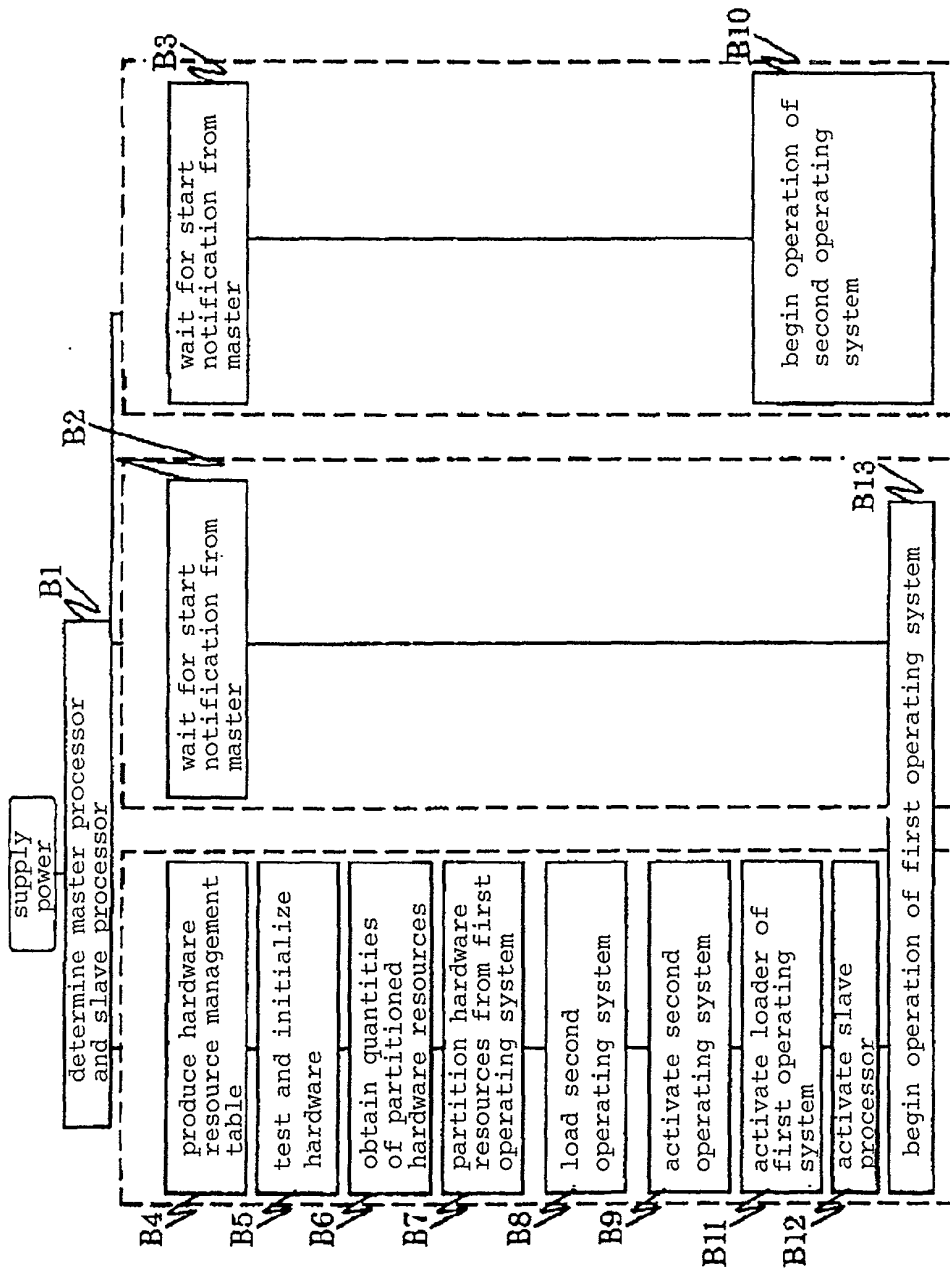


Fig. 11

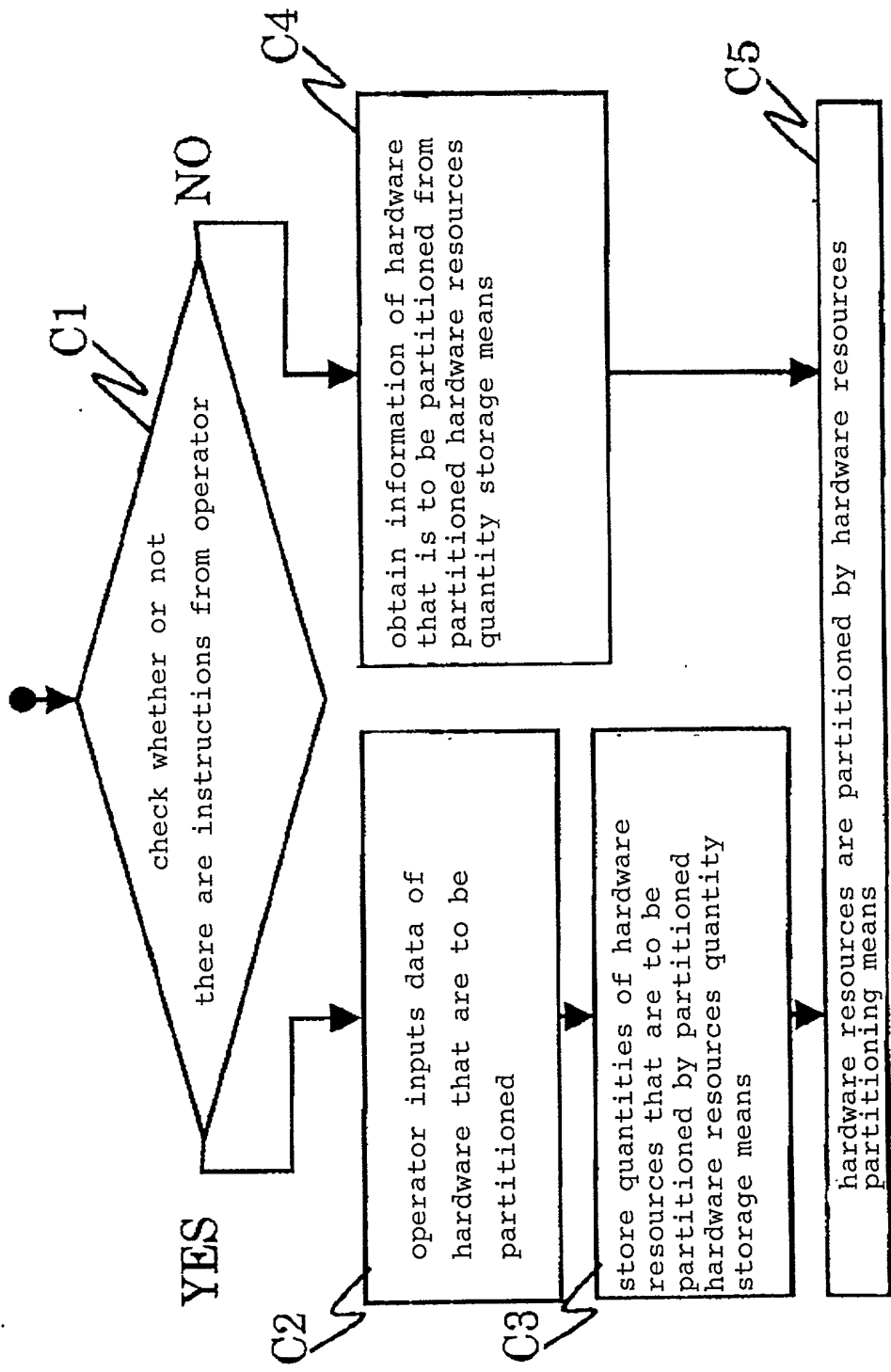
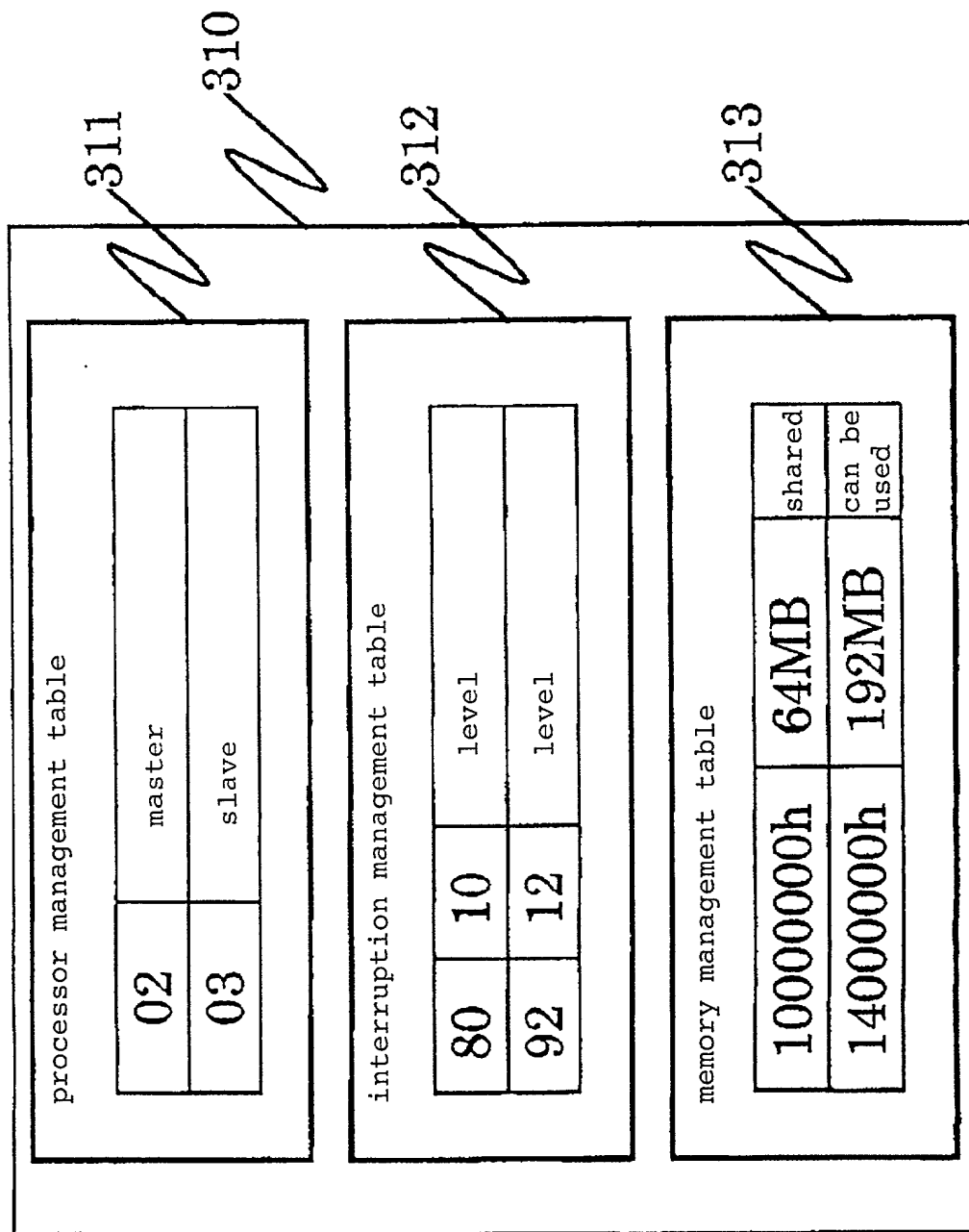


Fig. 12

hardware resources	quantities	110
processor entry for second operating system	2	111
interruption entry for second operating system	80	112
interruption entry for second operating system	92	113
memory entry for second operating system	192MB	114
shared memory entry for second operating system	64MB	115

Fig. 13



00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000

Fig. 14

400

start address	length	attribute
10000000h	64MB	shared

Fig. 15

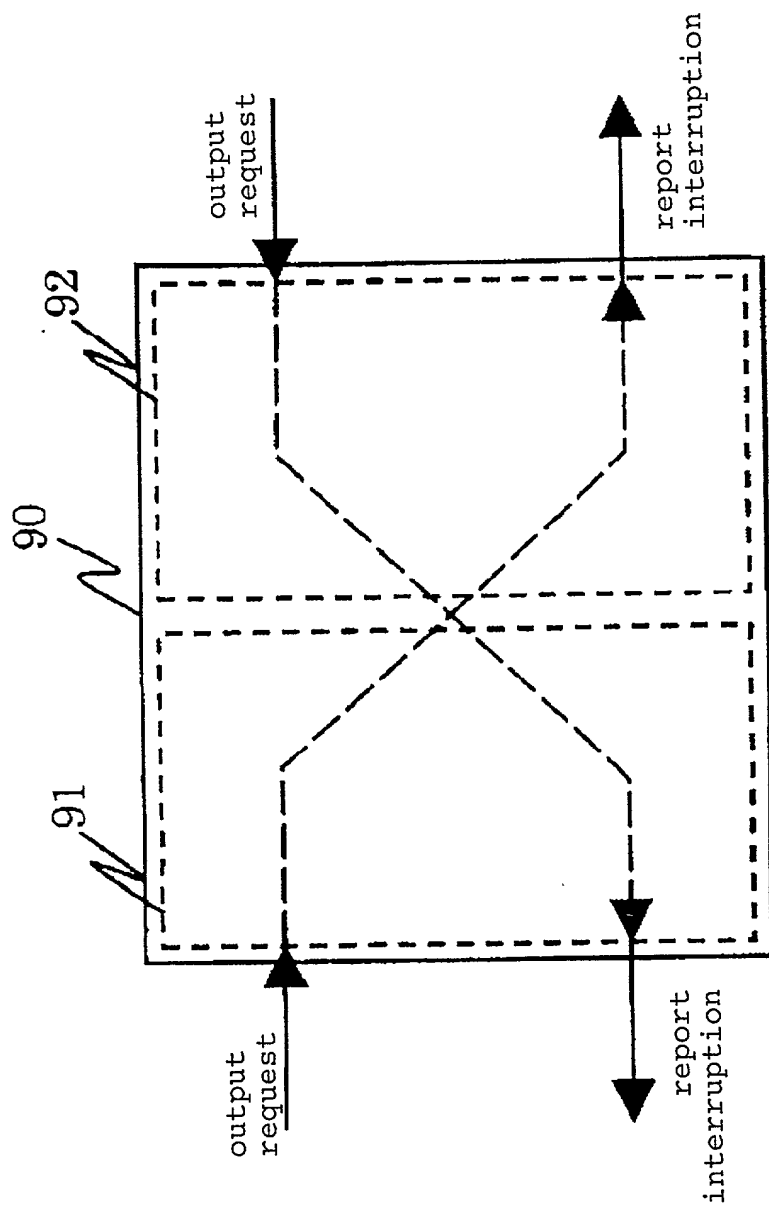


Fig. 16

240

1)

device ID	interruption number	report destination	attribute
50	01	all	edge trigger
60	05	all	edge trigger
80	10	all	level trigger
70	06	all	edge trigger
91	11	all	level trigger
92	12	all	level trigger

241

242

243

244

245

246



2)

device ID	interruption number	report destination	attribute
50	01	all	edge trigger
60	05	all	edge trigger
70	06	all	edge trigger
91	11	all	level trigger

241

242

244

245

Fig. 17

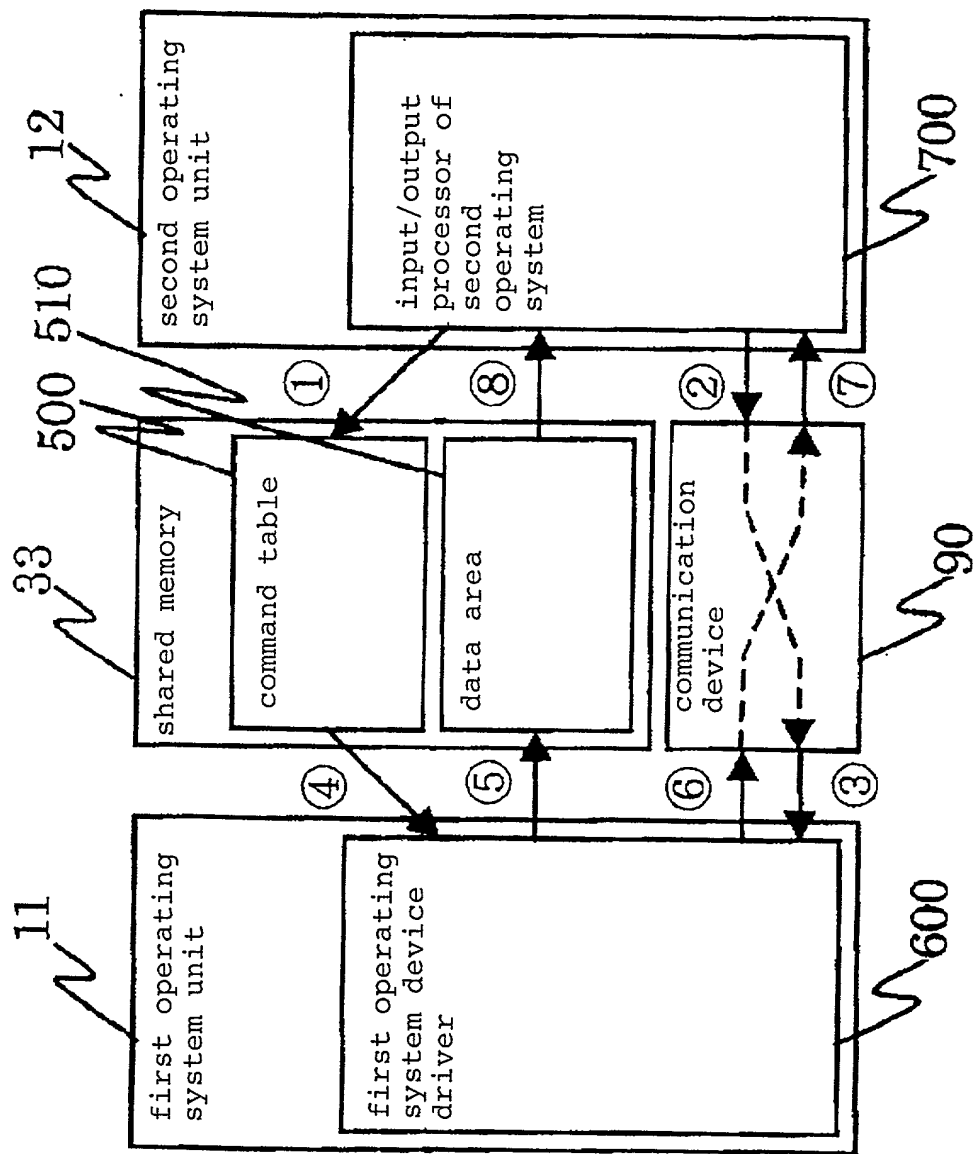


Fig. 18

